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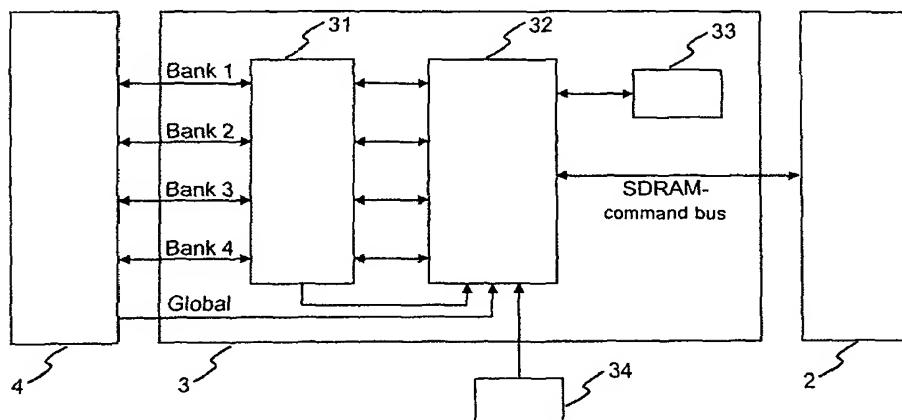
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(54) Title: MEMORY CONTROLLER



(57) **Abstract:** The present invention relates to a memory controller (1) for an IC with an external DRAM (2), where the external DRAM (2) has at least one memory bank (21, 22, 23, 24) and communicates with the IC via at least one channel (6, 7, 8). In line with the invention, the memory controller (1) has a command scheduler (3) which prioritizes the transmission of memory bank commands on the basis of a static priority allocation for commands and a dynamic priority allocation for channels.